Fig. 1

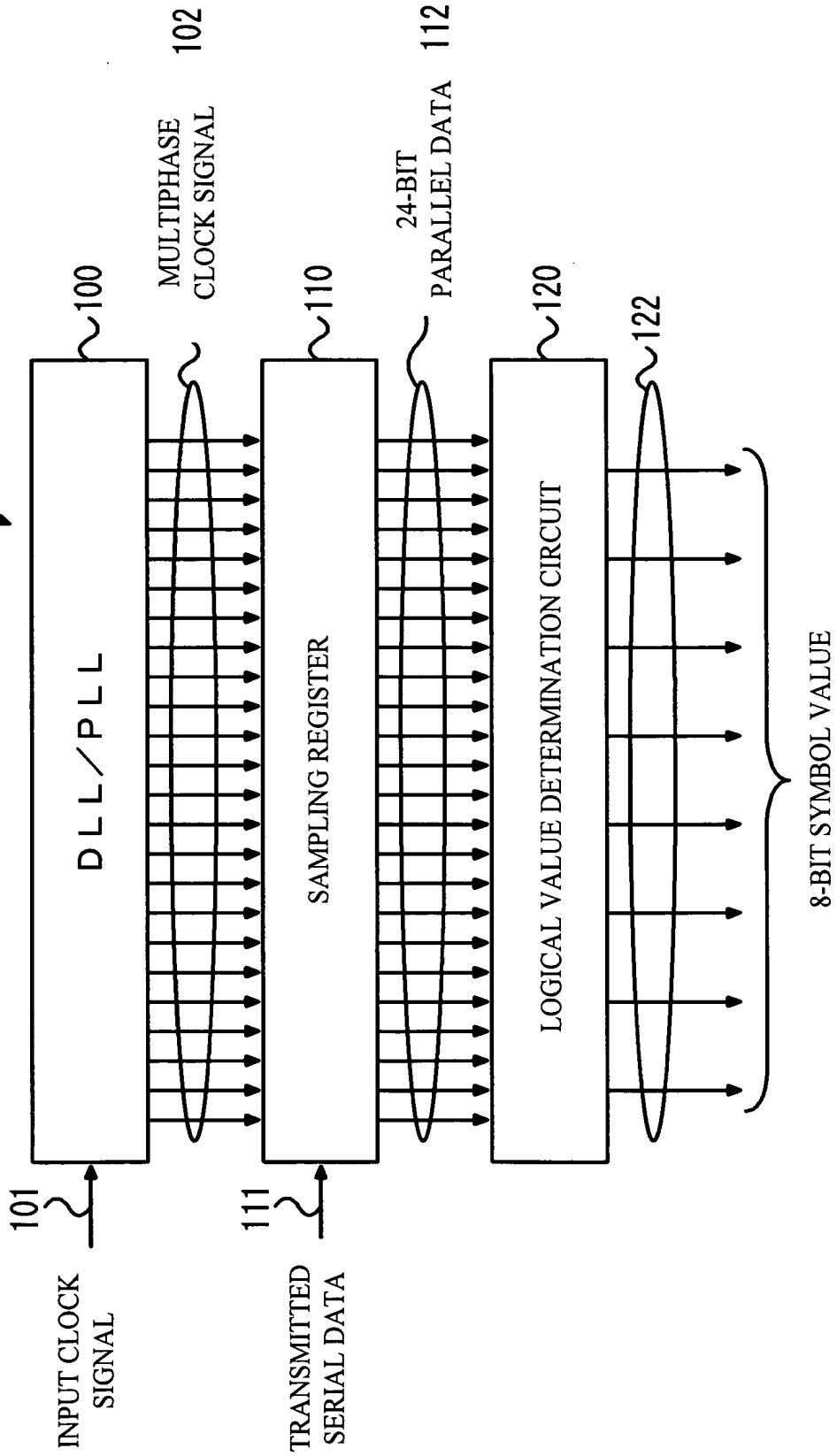

1000
100
DLL/PLL
101
INPUT CLOCK SIGNAL
102
MULTIPHASE CLOCK SIGNAL
110
SAMPLING REGISTER
111
TRANSMITTED SERIAL DATA
112
24-BIT PARALLEL DATA
120
LOGICAL VALUE DETERMINATION CIRCUIT
122
8-BIT SYMBOL VALUE

Fig. 2

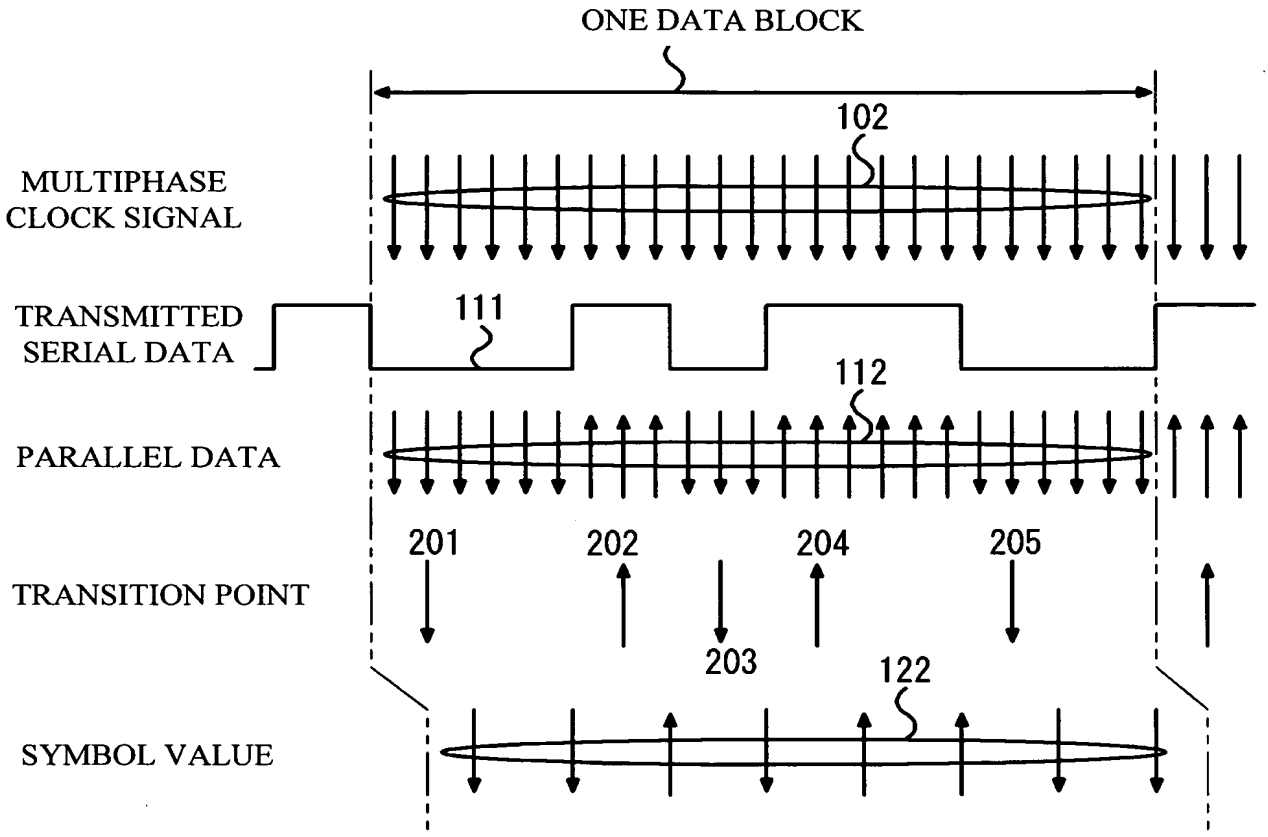

ONE DATA BLOCK
102
MULTIPHASE CLOCK SIGNAL
TRANSMITTED SERIAL DATA
111
112
PARALLEL DATA
201
202
204
205
TRANSITION POINT
203
122
SYMBOL VALUE

Fig. 3

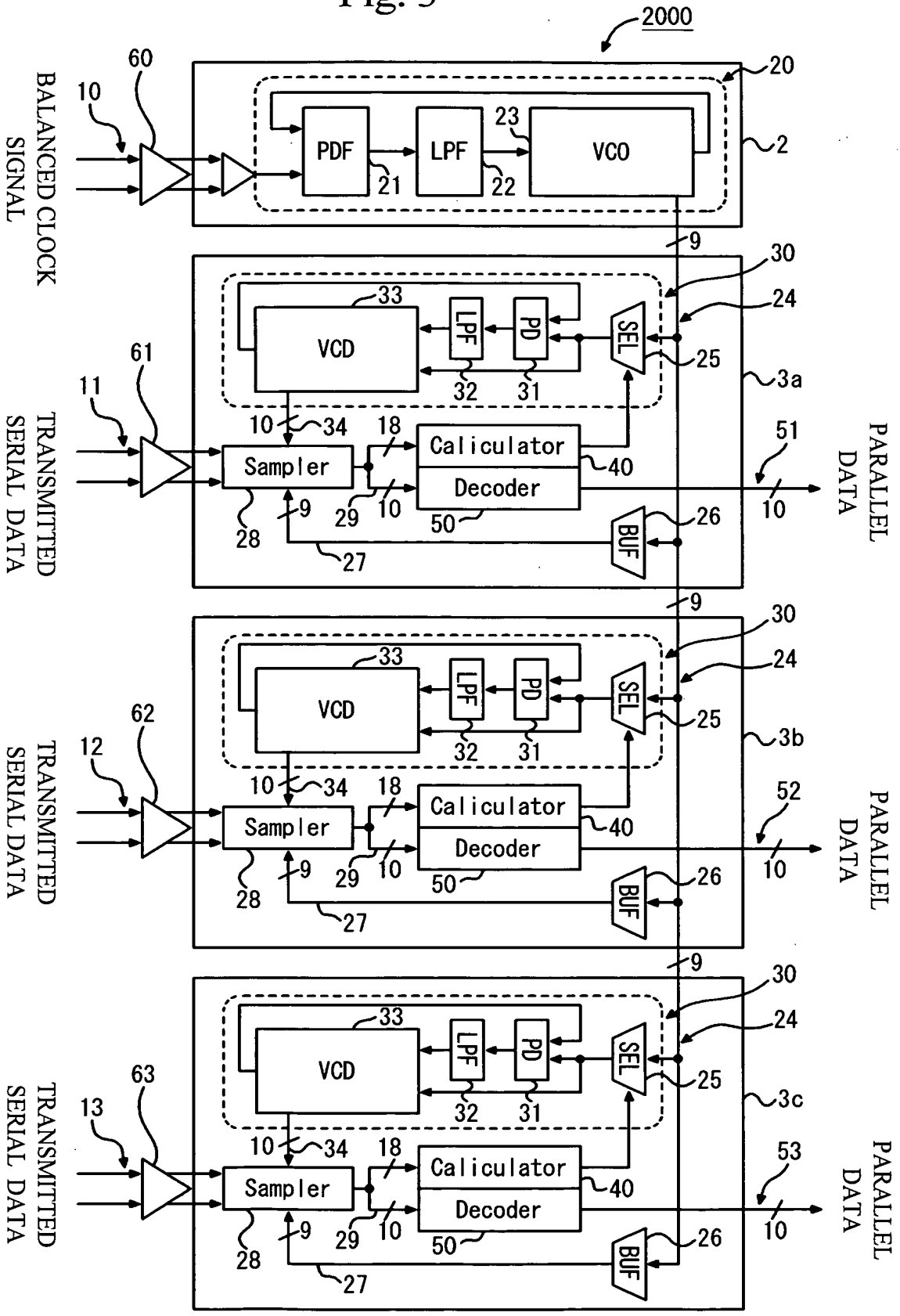

2000
BALANCED CLOCK SIGNAL
TRANSMITTED SERIAL DATA
TRANSMITTED SERIAL DATA
TRANSMITTED SERIAL DATA
PARALLEL DATA
PARALLEL DATA
PARALLEL DATA
PDF
LPF
VCO
VCD
PD
SEL
Sampler
Caliculator
Decoder
BUF
10
11
12
13
2
3a
3b
3c
9
18
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
40
50
51
52
53
60
61
62
63

Fig. 4

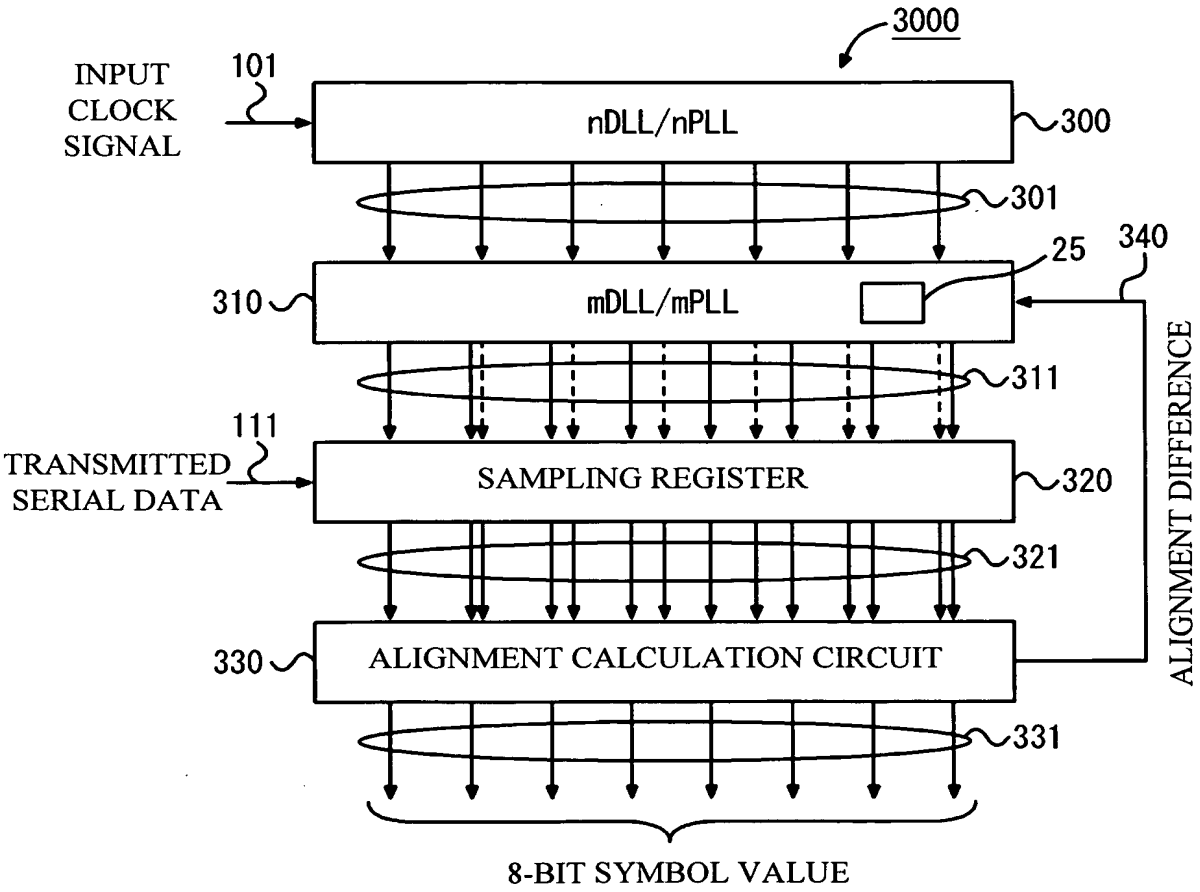

3000
INPUT CLOCK SIGNAL
101
nDLL/nPLL
300
301
25
340
310
mDLL/mPLL
311
111
TRANSMITTED SERIAL DATA
SAMPLING REGISTER
320
321
330
ALIGNMENT CALCULATION CIRCUIT
331
ALIGNMENT DIFFERENCE
8-BIT SYMBOL VALUE

Fig. 5

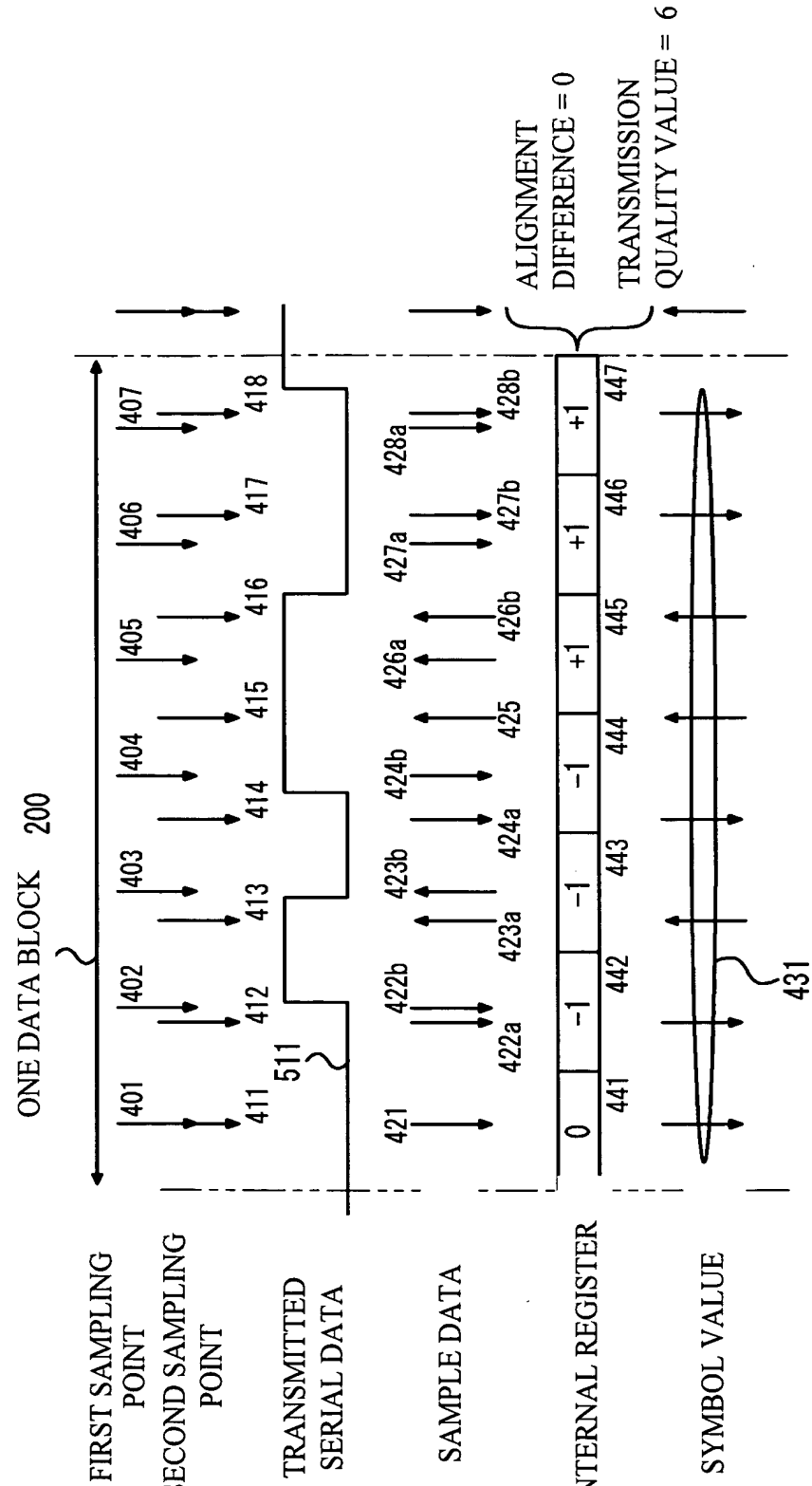

ONE DATA BLOCK 200
FIRST SAMPLING POINT
SECOND SAMPLING POINT
TRANSMITTED SERIAL DATA
SAMPLE DATA
INTERNAL REGISTER
SYMBOL VALUE
ALIGNMENT DIFFERENCE = 0
TRANSMISSION QUALITY VALUE = 6
401
402
403
404
405
406
407
411
412
413
414
415
416
417
418
421
422a
422b
423a
423b
424a
424b
425
426a
426b
427a
427b
428a
428b
441
442
443
444
445
446
447
511
431
0
-1
-1
-1
+1
+1
+1

Fig. 6

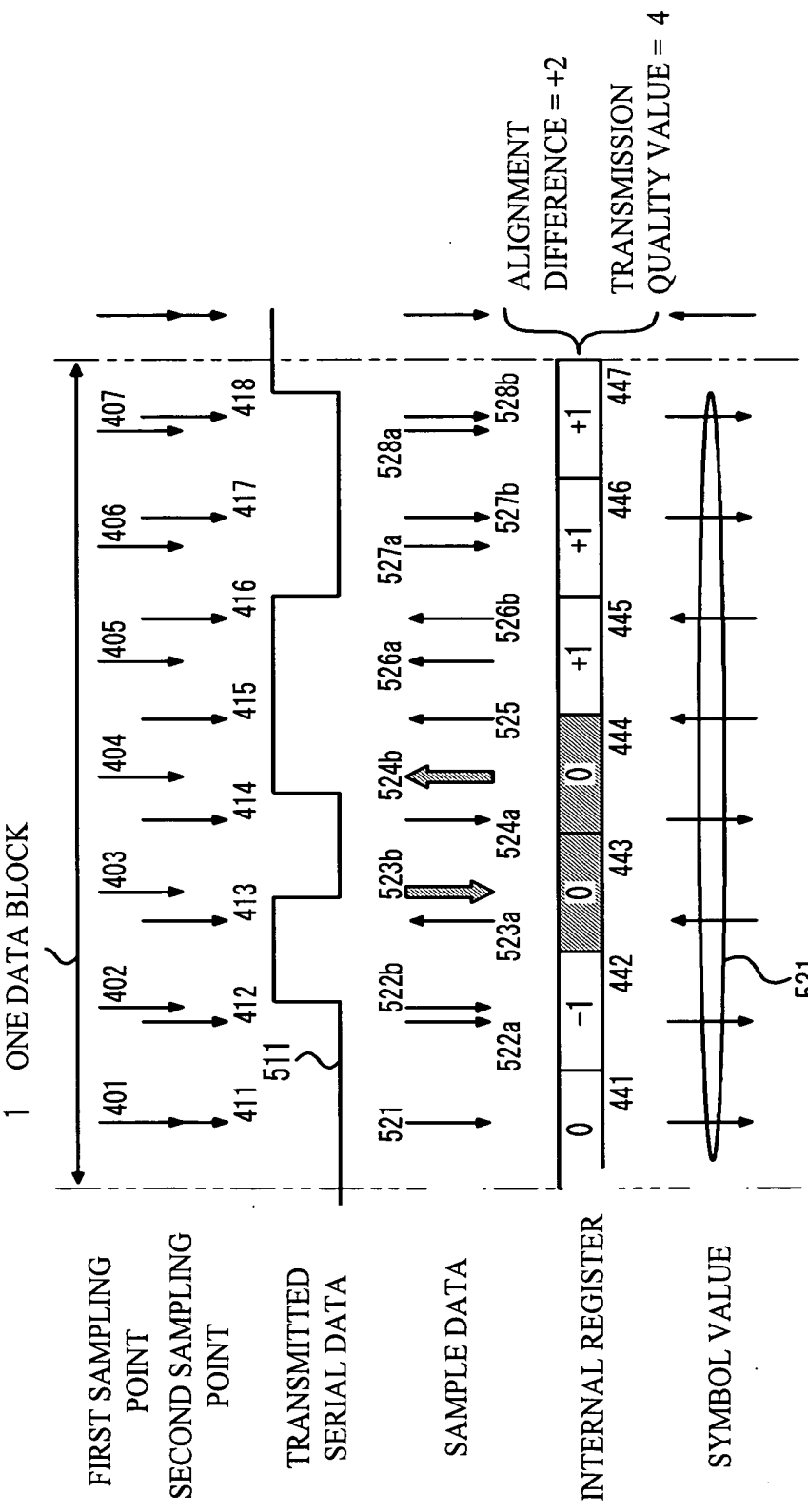

1 ONE DATA BLOCK
FIRST SAMPLING POINT
SECOND SAMPLING POINT
TRANSMITTED SERIAL DATA
SAMPLE DATA
INTERNAL REGISTER
SYMBOL VALUE
ALIGNMENT DIFFERENCE = +2
TRANSMISSION QUALITY VALUE = 4
401
402
403
404
405
406
407
411
412
413
414
415
416
417
418
511
521
522a
522b
523a
523b
524a
524b
525
526a
526b
527a
527b
528a
528b
441
442
443
444
445
446
447
0
-1
0
0
+1
+1
+1
531

Fig. 7

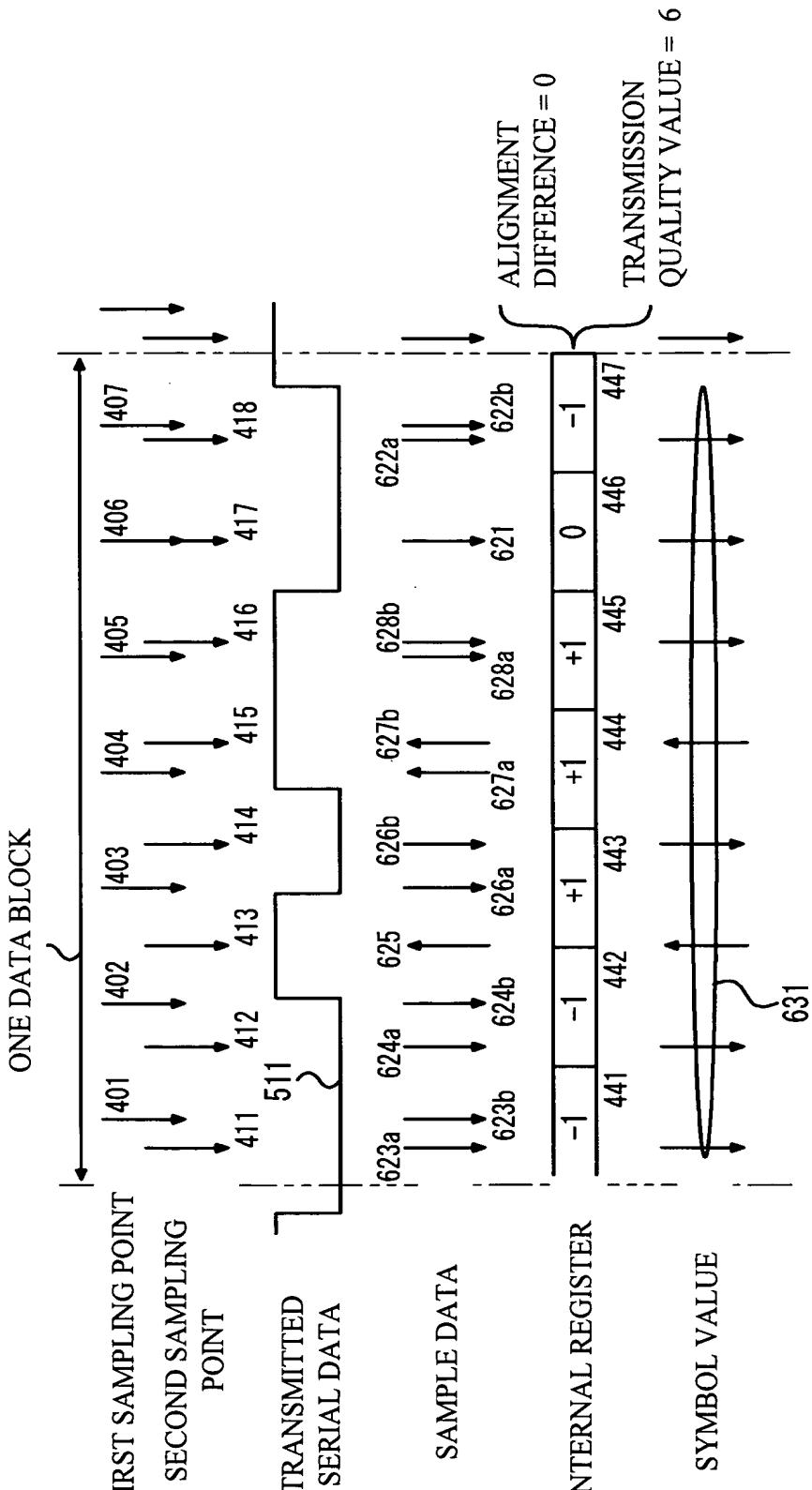

ONE DATA BLOCK
FIRST SAMPLING POINT
SECOND SAMPLING POINT
TRANSMITTED SERIAL DATA
SAMPLE DATA
INTERNAL REGISTER
SYMBOL VALUE
ALIGNMENT DIFFERENCE = 0
TRANSMISSION QUALITY VALUE = 6
401
402
403
404
405
406
407
411
412
413
414
415
416
417
418
511
623a
624a
625
626b
627b
628b
622a
621
622b
623b
624b
626a
627a
628a
-1
-1
+1
+1
+1
0
-1
441
442
443
444
445
446
447
631

Fig. 8A

This Invention (M/N sampling method)

m	n	m/n-1.0	# of CLKs	skew shift(deg)
8	5	0.60	10	27.00
8	6	0.33	12	15.00
8	7	0.14	14	6.43

Fig. 8B

Prior Art (X sampling method)

m	X	———	# of CLKs	skew shift(deg)
8	3	———	24	15.00
8	4	———	32	11.25

Fig. 9

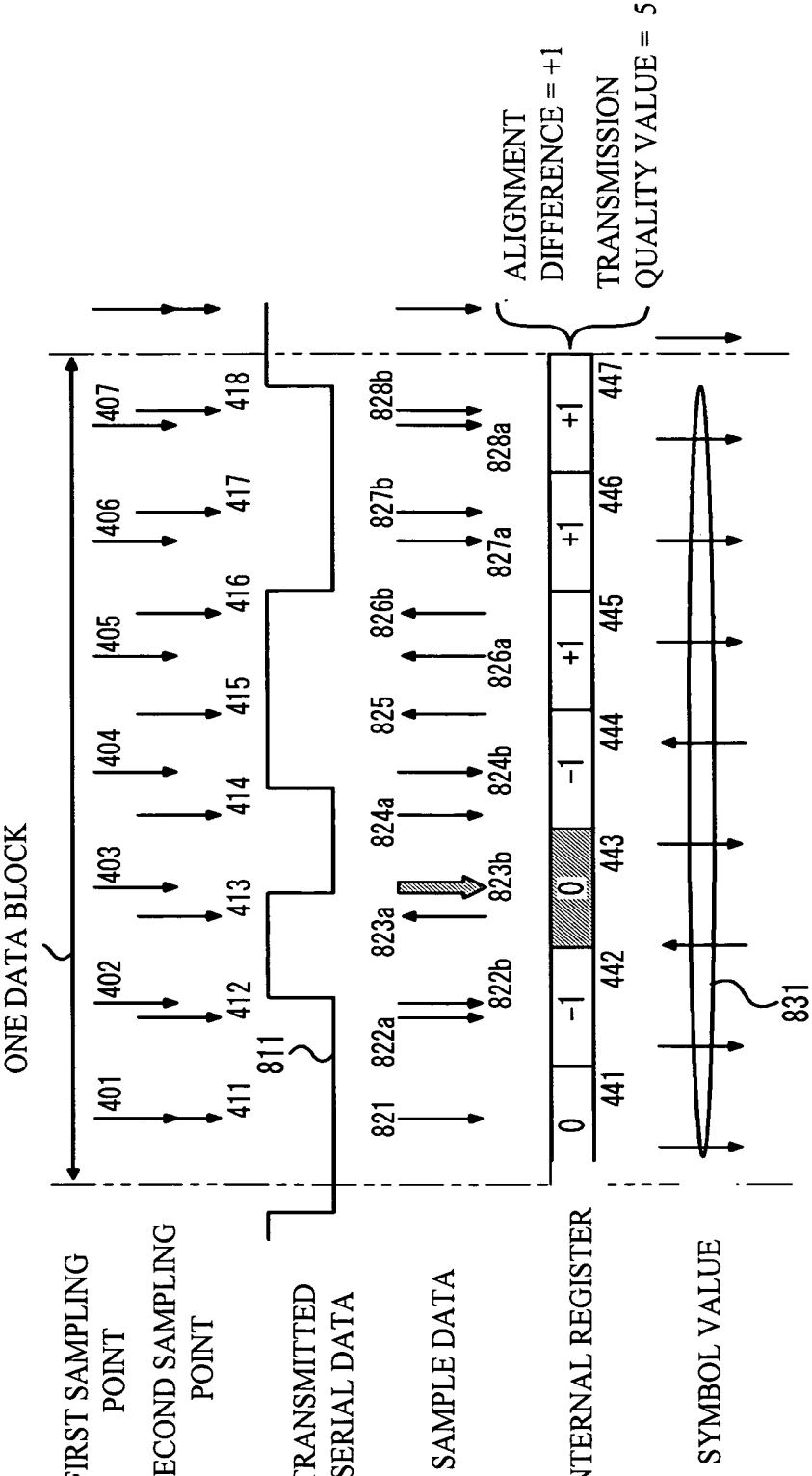

ONE DATA BLOCK
FIRST SAMPLING POINT
SECOND SAMPLING POINT
TRANSMITTED SERIAL DATA
SAMPLE DATA
INTERNAL REGISTER
SYMBOL VALUE
ALIGNMENT DIFFERENCE = +1
TRANSMISSION QUALITY VALUE = 5
401
402
403
404
405
406
407
411
412
413
414
415
416
417
418
811
821
822a
822b
823a
823b
824a
824b
825
826a
826b
827a
827b
828a
828b
441
442
443
444
445
446
447
0
-1
0
-1
+1
+1
+1
831

Fig. 10

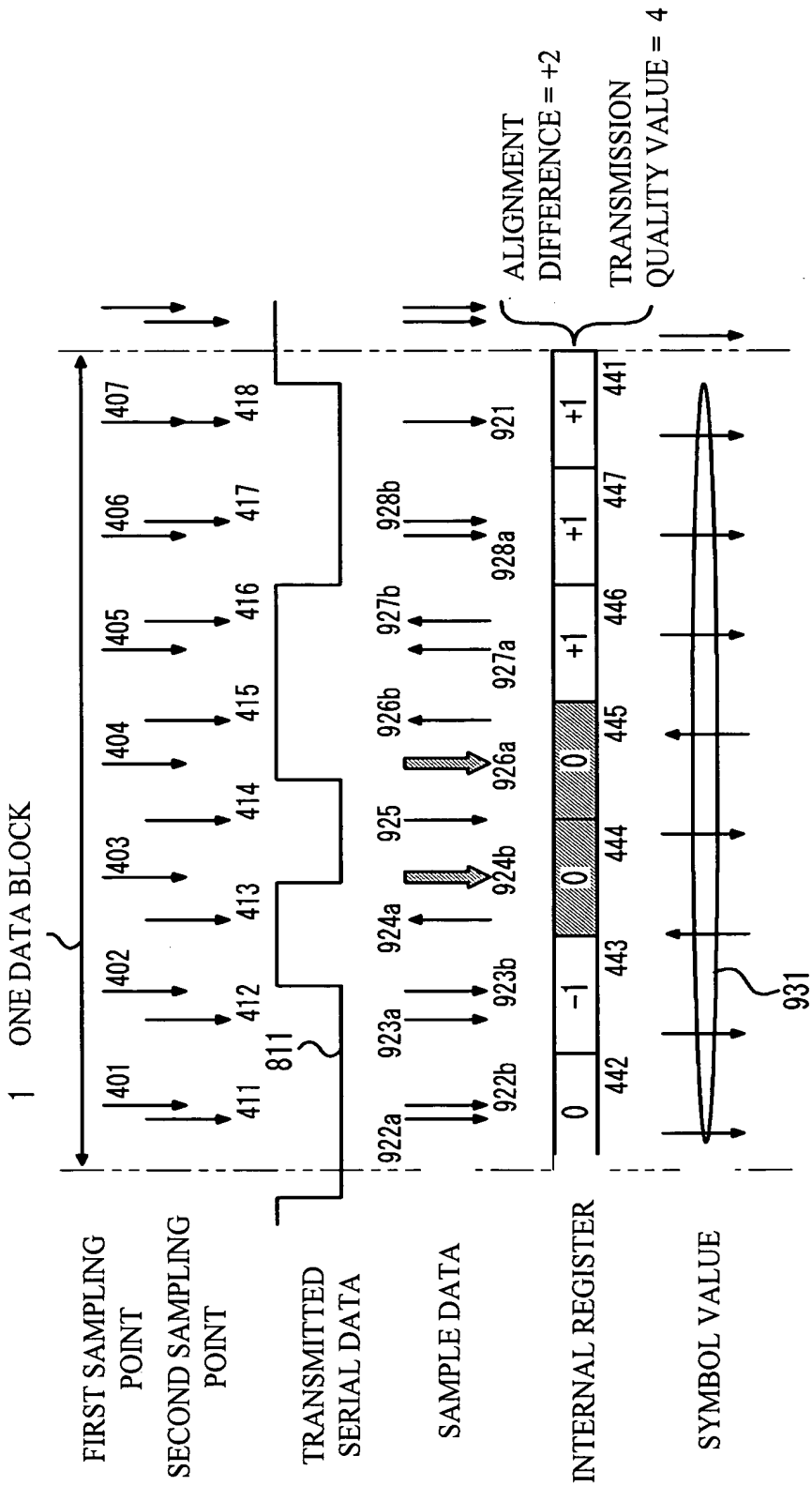

1 ONE DATA BLOCK
FIRST SAMPLING POINT
SECOND SAMPLING POINT
TRANSMITTED SERIAL DATA
SAMPLE DATA
INTERNAL REGISTER
SYMBOL VALUE
ALIGNMENT DIFFERENCE = +2
TRANSMISSION QUALITY VALUE = 4
401
402
403
404
405
406
407
411
412
413
414
415
416
417
418
811
922a
922b
923a
923b
924a
924b
925
926a
926b
927a
927b
928a
928b
921
0
-1
0
0
+1
+1
+1
441
442
443
444
445
446
447
931

Fig. 11

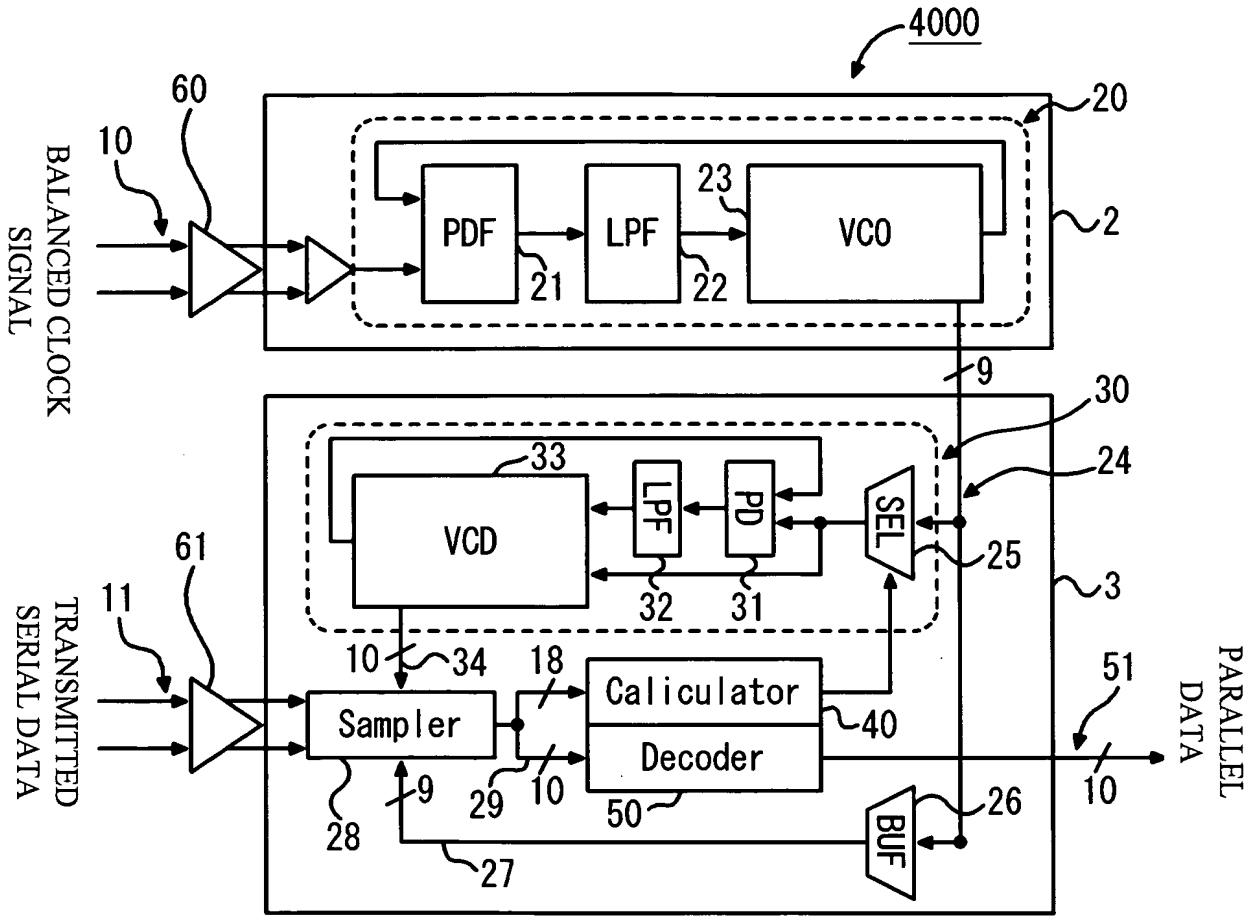

4000
60
10
BALANCED CLOCK SIGNAL
20
PDF
LPF
23
VCO
2
21
22
9
30
33
24
VCD
LPF
PD
SEL
61
25
11
TRANSMITTED SERIAL DATA
32
31
3
10
34
18
Caliculator
51
Sampler
40
Decoder
PARALLEL DATA
9
29
10
50
26
10
28
BUF
27

Fig. 12

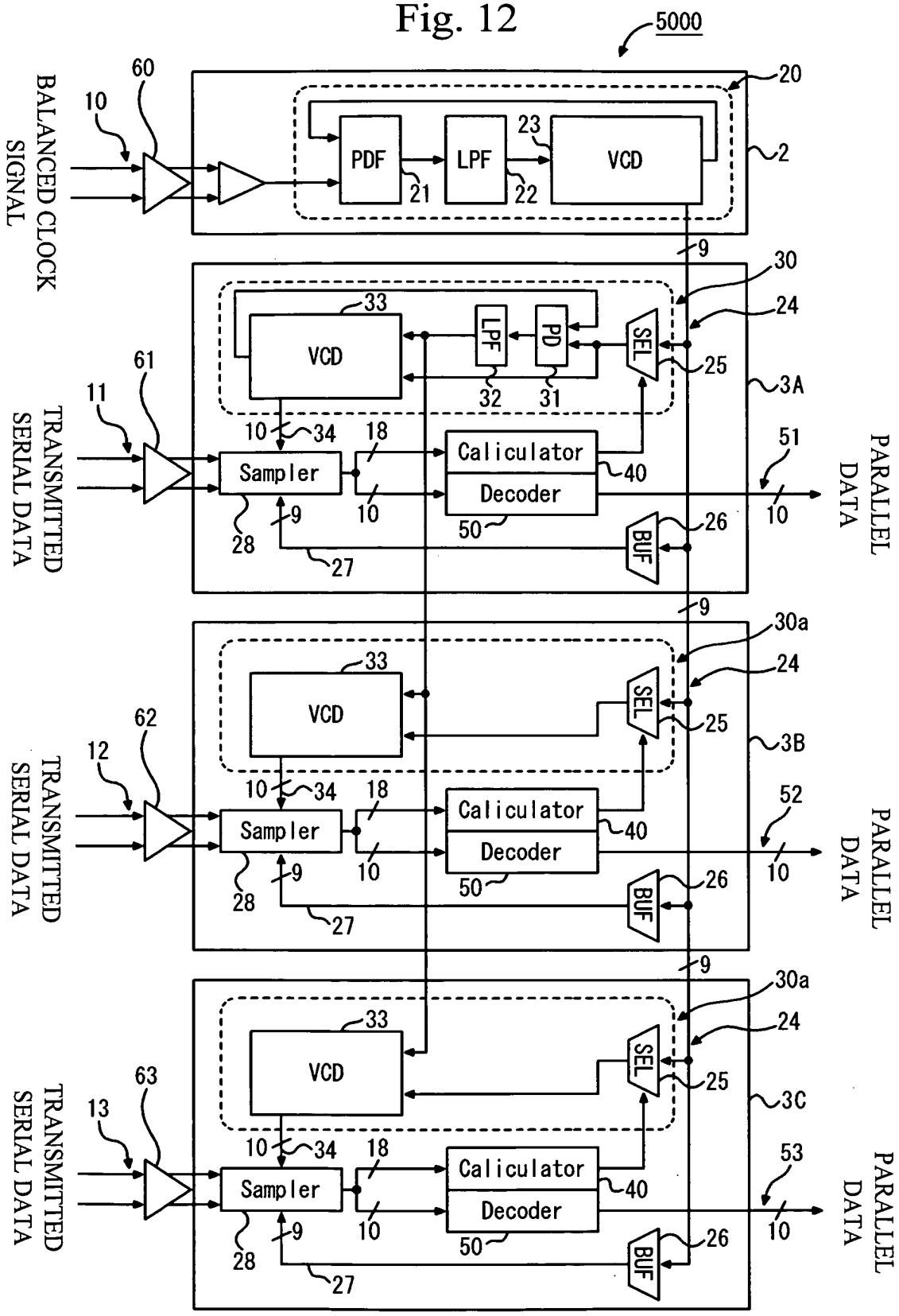

5000
BALANCED CLOCK SIGNAL
TRANSMITTED SERIAL DATA
TRANSMITTED SERIAL DATA
TRANSMITTED SERIAL DATA
PARALLEL DATA
PARALLEL DATA
PARALLEL DATA
PDF
LPF
VCD
PD
SEL
BUF
Sampler
Caliculator
Decoder
2
3A
3B
3C
9
10
11
12
13
18
20
21
22
23
24
25
26
27
28
30
30a
31
32
33
34
40
50
51
52
53
60
61
62
63

Fig. 13

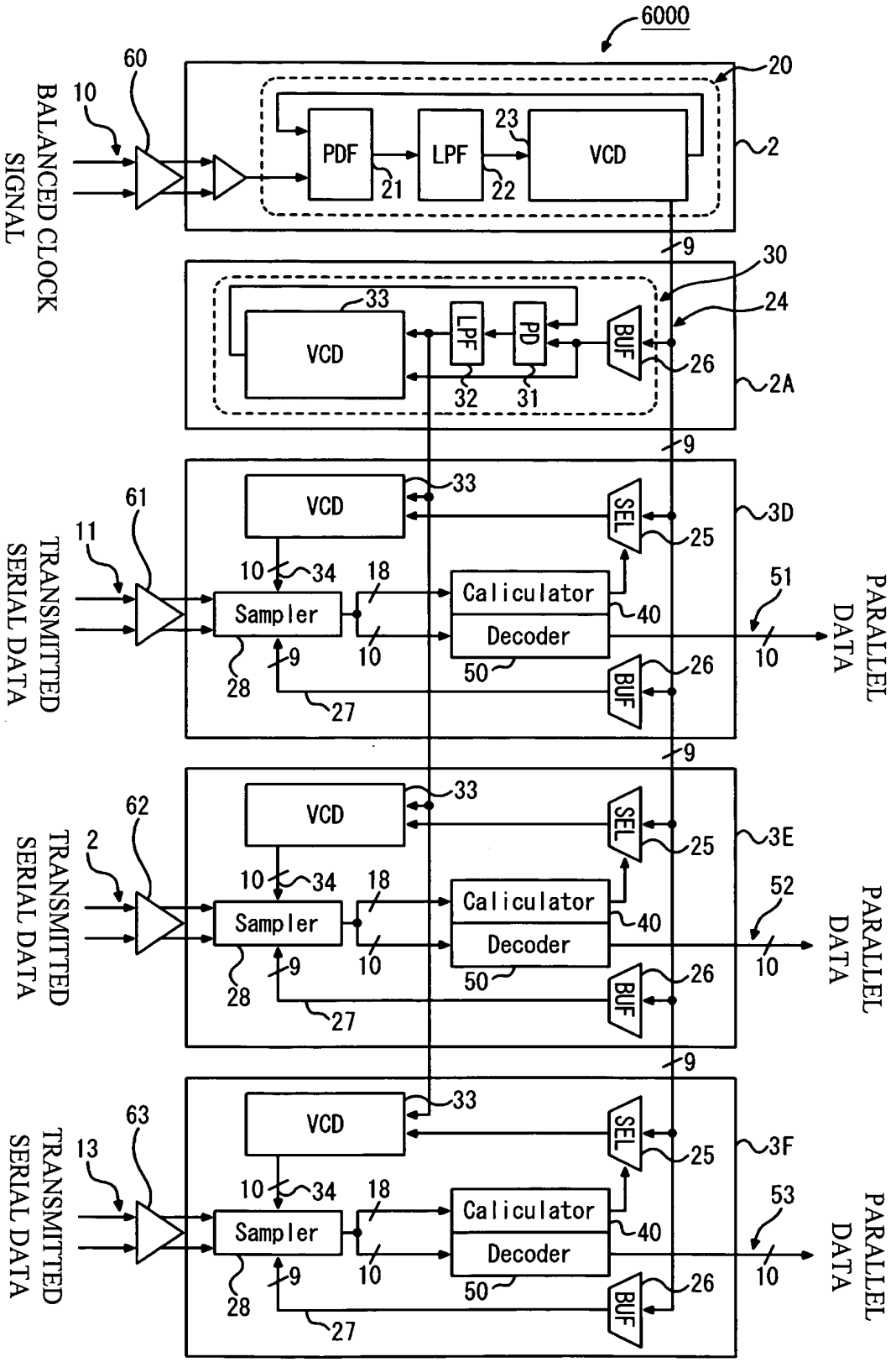
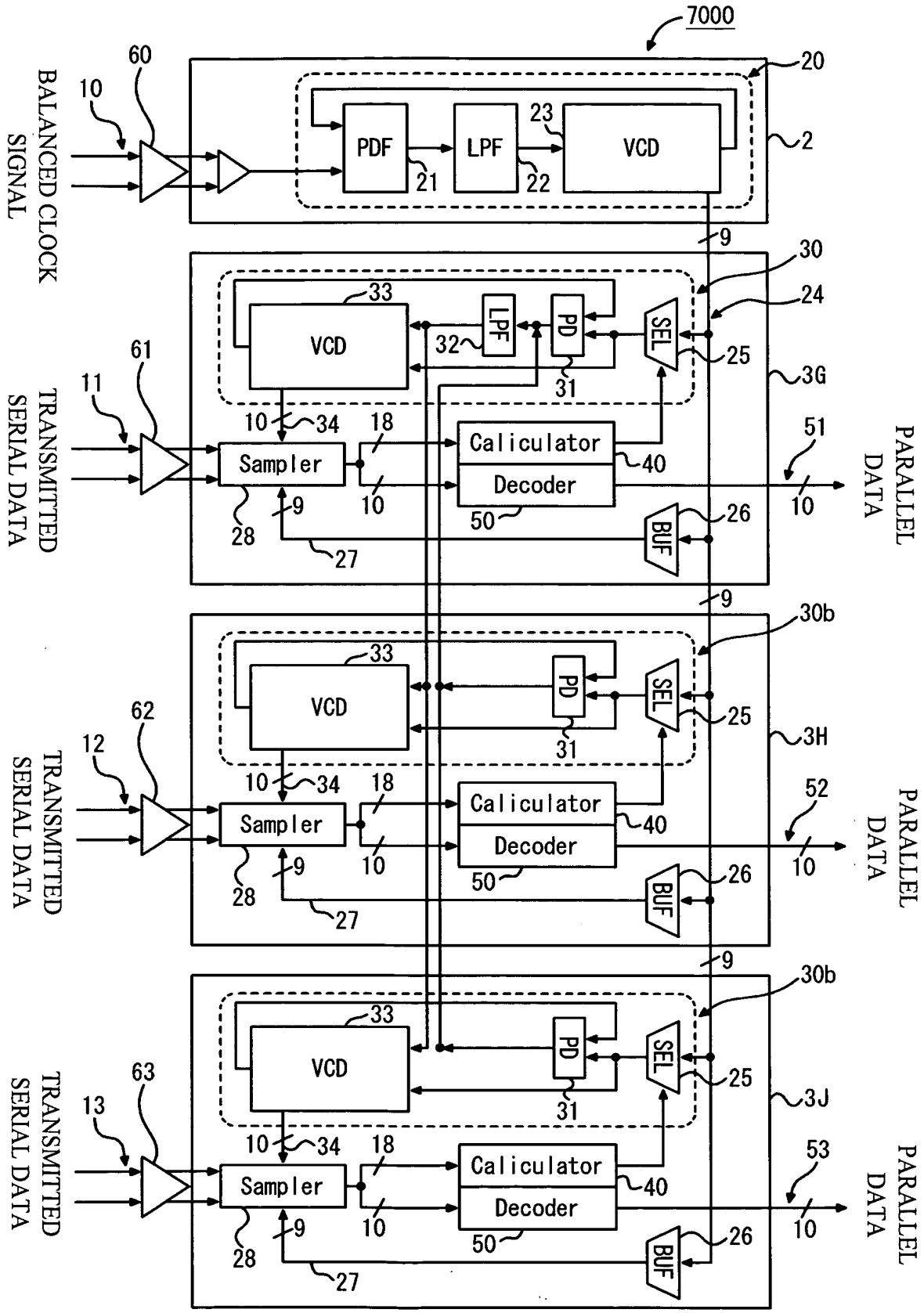

6000
BALANCED CLOCK SIGNAL
TRANSMITTED SERIAL DATA
TRANSMITTED SERIAL DATA
TRANSMITTED SERIAL DATA
PARALLEL DATA
PARALLEL DATA
PARALLEL DATA
PDF
LPF
VCD
PD
BUF
SEL
Sampler
Caliculator
Decoder
2
2A
3D
3E
3F

Fig. 14


7000
BALANCED CLOCK SIGNAL
TRANSMITTED SERIAL DATA
TRANSMITTED SERIAL DATA
TRANSMITTED SERIAL DATA
PARALLEL DATA
PARALLEL DATA
PARALLEL DATA
PDF
LPF
VCD
PD
SEL
BUF
Sampler
Caliculator
Decoder
10
11
12
13
2
3G
3H
3J
9
18
20
21
22
23
24
25
26
27
28
30
30b
31
32
33
34
40
50
51
52
53
60
61
62
63